

SOLID STATE IMAGING DEVICE

Field of the Invention

The present invention relates to a solid state imaging device which can be operated to provide an improved shutter function.

Background of the Invention

There are various basic CMOS pixel structures. One common type, with 3 transistors per pixel, is described in U.S. Patent No. 4,407,010 (referred to as the CMOS 3T pixel), and is illustrated in Figure 1 of the accompanying drawings. This is an efficient structure, wherein transistor M1 amplifies an output from the photodiode while positioned within the pixel. Transistor M2 resets the voltage on the pixel, and transistor M3 is a multiplex transistor.

Transistor M3 enables many pixels in a column to be wired together, and only one pixel is enabled at a time. The device Iload is typically a sense amplifier that provides a load for the source follower transistor M1, and also measures the output voltage.

The typical voltage on a photodiode is shown in Figure 2. At point 1, the pixel is reset by turning on transistor M2 which sets the voltage on the reverse-biased diode to a preset voltage (VRT). After this

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on the pixel and this reduces the amount of light reaching the photodiode. Transferring all the charge from Cpd to Csn is difficult to achieve. Special CMOS manufacturing techniques are often employed to change the structure of the photodiode Cpd or the transfer transistor M4. These manufacturing techniques are very costly since as they are non-standard and are also difficult to reliably achieve.

There are also some linear arrays (see Figure 5) with two rows of pixels which have separate electronics on both top and bottom. However, these structures are limited to a maximum of two rows. Other prior art in this area includes U.S. Patent Nos. 4,835,617; 5,576,762; 5,134,489; 5,122,881; 5,471,515, and European Patent WO 98/08079.

Summary of the Invention

An object of the present invention is to provide a solid state image sensor which, like the 3T sensor, can be manufactured by standard techniques, but which also is capable of providing a true electronic shutter.

The invention and preferred features thereof are defined in the appended Claims.

Briefly stated, the invention is based upon locating the readout electronics off the image plane of the device. In preferred forms of the invention, this is facilitated by connecting each pixel to its associated readout electronics via a multi-conductor signal bus.

Brief Description of the Drawings

Embodiments of the invention will now be

described, by way of example only, referring to the drawings in which:

Figures 1 to 5 illustrate the prior art as discussed above;

5 Figure 6 shows part of one column of an array structure embodying the invention;

Figure 7 is a timing diagram illustrating the operation of Figure 6;

10 Figure 8 shows a typical system layout of a sensor incorporating the circuitry of Figure 6;

Figure 9 shows one pixel and read-out circuitry of a modified version of Figure 6;

Figure 10 is a timing diagram illustrating the operation of Figure 9;

15 Figure 11 shows one pixel plus read-out circuitry of a further modification of Figure 6;

Figure 12 is a timing diagram illustrating the operation of Figure 11;

20 Figure 13 is a view similar to Figure 8 but showing a modified system layout; and

Figure 14 shows a preferred readout arrangement for the circuit of Figure 11.

Detailed Description of the Preferred Embodiments

25 A basic feature of the invention is to provide a storage node per pixel, and to avoid degrading the fill factor and hence light sensitivity, by locating the storage element away from the image plane. Referring to Figure 6, this embodiment has only two transistors, M1 and M2 per pixel, thus improving
30 the fill factor and sensitivity. The array is not multiplexed, and therefore there is no multiplex transistor in the pixel equivalent to M3 in Figure 1.

The switches S2-1, S2-2 will typically be implemented as MOSFET transistors. The current loads Iload are to ensure correct operation of sense transistor M1. Figure 6 shows only two pixels, but in a practical array there are several pixels in a column.

10 causing all the M2 transistors (M2_1, M2_2, etc.) to
conduct and the voltage Vpix on the photodiode to be
reset to Vrt. At a time later point 2 (see Figure 7),
all the S1 switches (S1_1, S1_2, etc.) are closed
simultaneously and the output of the sense transistors
15 (M1) are stored on the sense capacitors (Csn_1, Csn_2).
Subsequently (not shown), the signals on the sense
capacitors are readout sequentially by sequentially
closing switches S2 (S2_1, S2_2, etc.).

Figure 8 shows a typical layout of a system with an image array 12 and sample capacitor area 14. To simplify the drawing, a 6 x 6 pixel structure is shown but the array would typically be larger. The output from each pixel is wired (indicated by the X in Figure 8) to a different conductor of the signal bus 10. Each cell has a width A within the system.

The embodiment of Figures 6 to 8 shows signal bus lines planar with the image plane, i.e., using the same conductor layer. One improvement (not shown) is to stack the conductors, that is, to use different
30 conductive layers. This reduces the amount of metal covering the pixel and thus improves the amount of light collected by the pixel.

The system described in Figure 6 is area and

cost efficient, but it suffers from a fixed pattern noise in the form of brightness variations on the picture. This is due to the varying amount of threshold voltage of transistors M1 over the array.

- 5 These variations are a normal part of the CMOS manufacturing process. A practical way of cancelling this offset is to measure, on a per-pixel basis, the reset voltage after the source follower.

Referring to Figures 9 and 10, this is
10 achieved by closing switch S3 (Figure 9) immediately after the end of the reset pulse (2 in Figure 10). This signal is then stored on Cres, and switch S3 is opened. For a period of time (3 in Figure 10), the pixel collects light and the photo-charge discharges
15 the photodiode. At the end of this period (4 in Figure 10) the signal is sampled on Csn. During image readout (5 in Figure 10), switches S2 and S4 are closed simultaneously and both the signal and reset values are output onto the output signal and reset value
20 conductors. The threshold voltage can then be compensated by subtracting the reset value from the output signal.

This technique is similar to that used in U.S. Patent No. 5,122,881 but is modified to deal with
25 the present situation where no multiplex transistor is present.

Although the technique described previously (Figure 9) cancels the offset, it degrades the rate at which the system can operate since it is not possible
30 to perform image acquisition and readout simultaneously. This is because the reset signal (2 in Figure 10) occurs at the start of an image acquisition, but is required during readout. A new acquisition is

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The solution to this problem is shown in Figure 11. An extra capacitor per pixel is used to enable simultaneous image acquisition and readout.

At this time the system has collected a complete set of reset and image values and is ready to readout. Before this occurs, the next acquisition cycle starts. At point 4, Vrst goes high causing all the M2s in the array to conduct for resetting the photodiodes in the array. As soon as this is complete, (point 5) S4 goes high enabling CresB to sample the reset value of the pixel. As the image array collects light, the pixels' capacitors are accessed sequentially. At point 6, S2 is closed to output the image value Vsn stored on Csn onto the output signal conductor. For this sequence of images, S4 is closed to output the reset value Vres stored on CresA onto the reset value A conductor. The image array collects light until time 7 when the voltage corresponding to the pixel's exposure to light is collected. S1 is closed and the voltage is stored on the pixel's Csn.

At this time the system has collected another

The system continues to operate using the sequence described above. The important feature to note in Figure 12 is that Vsn is able to be output on each frame.

An improved layout is shown in Figure 13.

25 This architecture has sample capacitors 14A and 14B at the top and bottom of the array 12. There are now two signal buses 10A and 10B divided in the center, and the cell width B is equal to $1/3$ of a pixel. There are two advantages. The fewer signal bus conductors running

30 across each pixel requires less metal, and hence, there is less obstruction of the pixel (i.e, a higher fill-factor) and hence greater sensitivity from the pixel. As the array is divided into two parts, the sample

capacitors are shared top and bottom, resulting in twice the width available.

The following Table 1 illustrates the advantages.

Table 1

5	Layout	Column Width	Pixel Array	Pixel Size	Image Plane	Imaging Area
	Figure 8	2 μ m	100x100	200 μ m x 200 μ m	200mm x 200mm	400m ²
	Figure 13	2 μ m	100x100	100 μ m x 100 μ m	100mm x 10mm	100m ²

As can be seen in the final column, the improved layout technique of Figure 13 produces a four-
10 fold increase in area, and hence a corresponding reduction in cost per unit area.

Turning to Figure 14, a preferred scheme for measuring and amplifying the two output signals will now be described. Associated with the switches S2, S4,
15 S6 and the conductors output signal 18, reset value A 20, and reset value B 22, are unwanted stray capacitances. As the array size increases, the number of pixels, and therefore, the number of switches increases. The cumulation of all these switches can
20 produce an unwanted capacitance roughly equal to that of the sampling capacitances. When the signals are read out (switches S2/S4/S6 closed), part of the charge stored on the capacitors Csn/CresA/CresB is used to charge the stray capacitors. This problem is known as
25 charge sharing. This can easily be 50% to 70% of the signal, and reduces the output swing to 1/2 or 1/4 of the true signal.

Using a differential, charge sensitive amplifier 16 as shown in Figure 14, charge sharing is
30 avoided. Before the signal is read out, the switches

S7, S8 are closed and the amplifier 16 is put into its common mode reset state. This discharges the capacitors Cf1, Cf2 on the feedback of the operational amplifier 16 and forces the conductors 18, 20, 22 to the common mode voltage. Switches S7/S8 are opened and S2, S4 (or S6) are then closed.

The nature of the operational amplifier is to ensure that its input remains at the common mode voltage. By doing so there is no change in the voltage on the lines 18, 20 and 22 and so there can be no loss of charge. During the readout, the voltages on Csn, CresA, CresB are also set to the common mode voltage. The change in voltage from that which was measured off the array requires a current to flow. This comes from the output of the op-amp 16 via the feedback capacitors Cf1, Cf2. For correct operation (symmetrical operation) the capacitance of Cf1=Cf2 and Csn=CresA=CresB. Hence:

$$\text{Out1-Out2}=(\text{Vsignal} - \text{Vreset})\times\text{Csn}/\text{Cf1}$$

Modifications and improvements may be made to the foregoing within the scope of the invention.